[54] HIGH SPEED DIGITAL SIGNAL FRAMER-DEMULTIPLEXER

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[58] Field of Search 370/106, 105, 100; 375/114, 116

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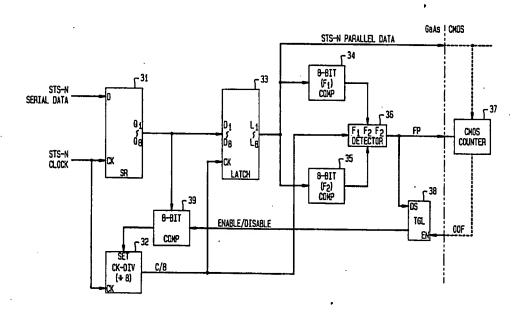|			
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[57] ABSTRACT

A framer-demultiplexer circuit provides means for reducing the high serial bit-stream rate of byte-interleaved low level signal frame structures proposed by the Synchronous Optical Network (SONET) signal hierarchy to speeds which can be processed with low-power low-cost CMOS VLSI technology, while establishing and maintaining basic byte integrity. In this circuitry the incoming high-rate serial bit stream is divided alternately between shift registers 43, 44 under the control of a single high-precision clock-division circuit to provide a multi-bit formatting that enables parallel delivery of stage bytes with the multifold reduction in transmission to a rate within the processing capabilities of CMOs devices. Necessary synchronization of the register and latching elements of the circuit with the incoming bit stream is effected through use of comparator means 62, 64 which detect key bit patterns within the standard framing bytes for controlling the phases of the bit-distribution and byte out-latch clocks 41, 48. Additional comparator circuitry 34, 35, 36 employs framing byte sequences established during synchronous byte output to detect and signal the occurrence of frame structure benchmarks from which data-processing CMOS circuitry can determine the boundaries of data bytes within the parallel byte output from the demultiplexed frame. The phase-control bit sequence comparator circuitry 62, 64 is disabled during periods of satisfactory frame processing, but is reactivated upon the detection of framing sequence error to provide resynchronization in order to ensure recovery of properly restaged data bytes.

21 Claims, 5 Drawing Sheets